Claims

[c1] A flip-flop comprising:
a first latch adapted to be coupled to a first power supply; and
a second latch coupled to the first latch and adapted to be coupled to a second power supply, wherein the first and second power supplies are independently controllable to minimize power consumption when the flip-flop is in a power saving mode.

[c2] The flip-flop of claim 1 wherein, in a power saving mode, the voltage of at least one of the first and second power supplies is reduced.

[c3] The flip-flop of claim 1 wherein, in a power saving mode, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

[c4] The flip-flop of claim 1 wherein the first latch is a master latch.

[c5] The flip-flop of claim 1 wherein the second latch is a slave latch.

[c6] The flip-flop of claim 1 further comprising a first clock coupled to the first latch and a second clock coupled to the second latch.

[c7] The flip-flop of claim 6 wherein the first clock and the second clock are free running.

[c8] The flip-flop of claim 6 wherein the first clock is gated and the second clock is free running.

[c9] The flip-flop of claim 6 wherein the first clock is free running and the second clock is gated.

[c10] The flip-flop of claim 6 wherein the first clock is gated and the second clock is gated.

[c11] A flip-flop comprising:
a first latch adapted to be coupled to a first power supply, the first latch

for receiving at least one bit;

a second latch coupled to the first latch and adapted to be coupled to a second power supply, the second latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized to reduce power consumption; and

a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a clock to the multiplexor is active and for outputting the at least one bit from the second latch when the clock is inactive, wherein the first and second power supplies are independently controllable.

[c12] The flip-flop of claim 11, wherein the multiplexor is a shunt multiplexor.

[c13] The flip-flop of claim 11 wherein a first clock causes the at least one bit to be provided to the first latch.

[c14] The flip-flop of claim 11 wherein the first latch is a master latch.

[c15] The flip-flop of claim 14 wherein the second latch is a slave latch.

[c16] The flip-flop of claim 15 which includes a restore mechanism which multiplexes the data and an output of the slave latch to enable recovery of the state of the contents of the master latch.

[c17] The flip-flop of claim 15 which includes a state saving latch which is coupled to the second power supply and is only activated upon detection of standby power saving mode.

[c18] The flip-flop of claim 1 wherein, in a power saving mode, the voltage of at least one of the first and second power supplies is reduced.

[c19] The flip-flop of claim 1 wherein, in a power saving mode, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

[c20] A flip-flop comprising:

a master latch adapted to be coupled to a first power supply, the master latch for receiving at least one bit; and

a slave latch coupled to the master latch and adapted to a second power supply, the slave latch for storing the at least one bit from the master latch wherein the size of the latch is minimized to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a clock to the multiplexor is active and for outputting the at least one bit from the slave latch when the clock is inactive, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

[c21] The flip-flop of claim 20 which includes a restore mechanism which multiplexes the data and an output of the slave latch to enable recovery of the state of the contents of the master latch.

[c22] The flip-flop of claim 20 which includes a state saving latch which is coupled to the second power supply and is only activated upon detection of standby power saving mode.

[c23]

A flip-flop comprising:

a master latch adapted to be coupled to a first power supply, the master latch for receiving at least one bit; and

a slave latch coupled to the master latch and adapted to a second power supply, the slave latch for storing the at least one bit from the master latch wherein the size of the latch is minimized to reduce power consumption;

a shunt multiplexor coupled to the master latch and to the slave latch for computing the at least one bit from the master latch when a clock to the multiplexor is active and for outputting the at least one bit from the slave latch when the clock is inactive, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a

voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts;

a restore mechanism which multiplexes the data and an output of the slave latch to enable recovery of the state of the contents of the master latch; and

a state saving latch which is coupled to the second power supply and is only activated upon detection of the power saving mode.

[c24] A method for minimizing the power consumption of a flip-flop, the flip-flop including a first latch and a second latch coupled thereto; the method comprising the steps of:

(a) providing a first independently controllable power supply coupled to the first latch;

(b) providing a second independently controllable power supply coupled to the second latch; and

(c) reducing the voltage of at least one of the first and second power supplies responsive to the detection of a power saving mode.

[c25] The method of claim 24 wherein, in a power saving mode, the voltage of the power supply coupled to the latch which contains contents to be preserved is reduced to a voltage to preserve the state of the contents and the other power supply is reduced to substantially zero volts.

[c26] The method of claim 24 wherein the first latch is a master latch.

[c27] The method of claim 26 wherein the second latch is a slave latch.

[c28] The method of claim 27 further comprising a first clock coupled to the first latch and a second clock coupled to the second latch.

[c29] A method for returning normal mode from power saving mode to preserve the contents in a flip-flop, the flip-flop including a first latch and a second latch coupled thereto, the method comprising the steps of:

(a) providing a first independently controllable power supply coupled to the master latch;

(b) providing a second independently controlling power supply coupled to

the second latch, wherein the at least one of the first and second power supplies is at substantially zero volts and the other of the first and second power supplies is at a reduced voltage such that the state of the contents in the associated latch is preserved;

(c) detecting the normal mode; and

(d) restoring the first and second power supplies to full values.